FIG. 1A

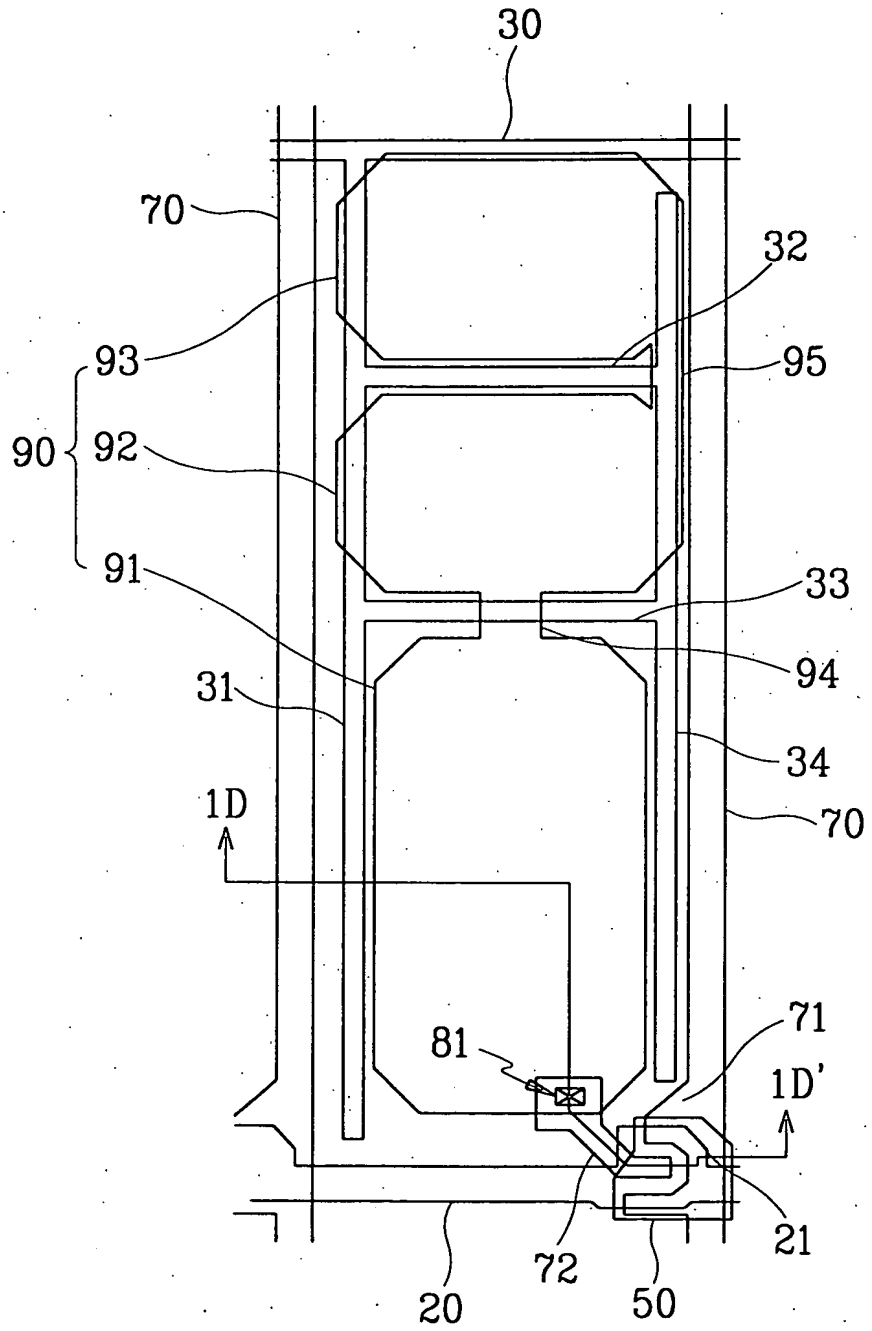


FIG. 1B

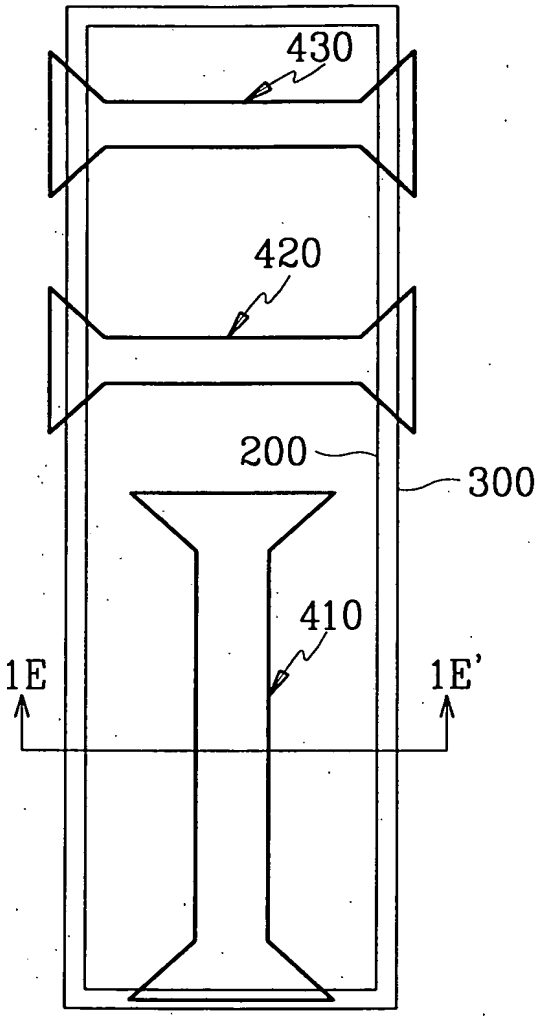


FIG. 1C

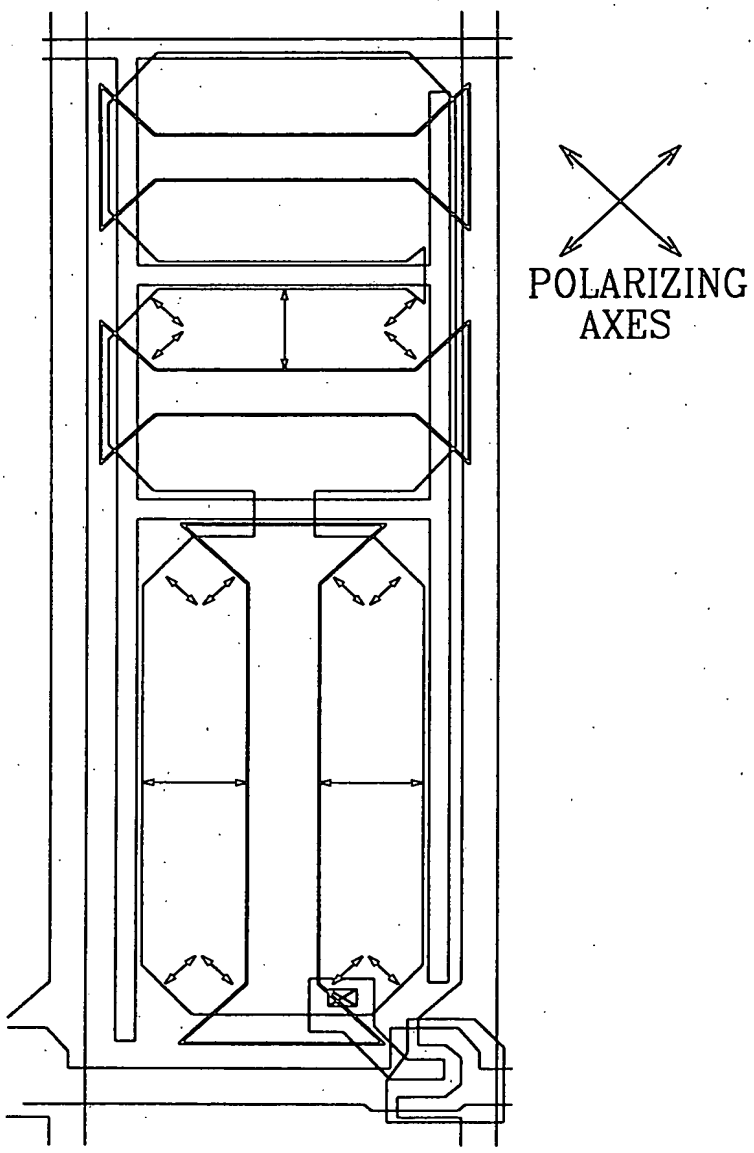


FIG. 1D

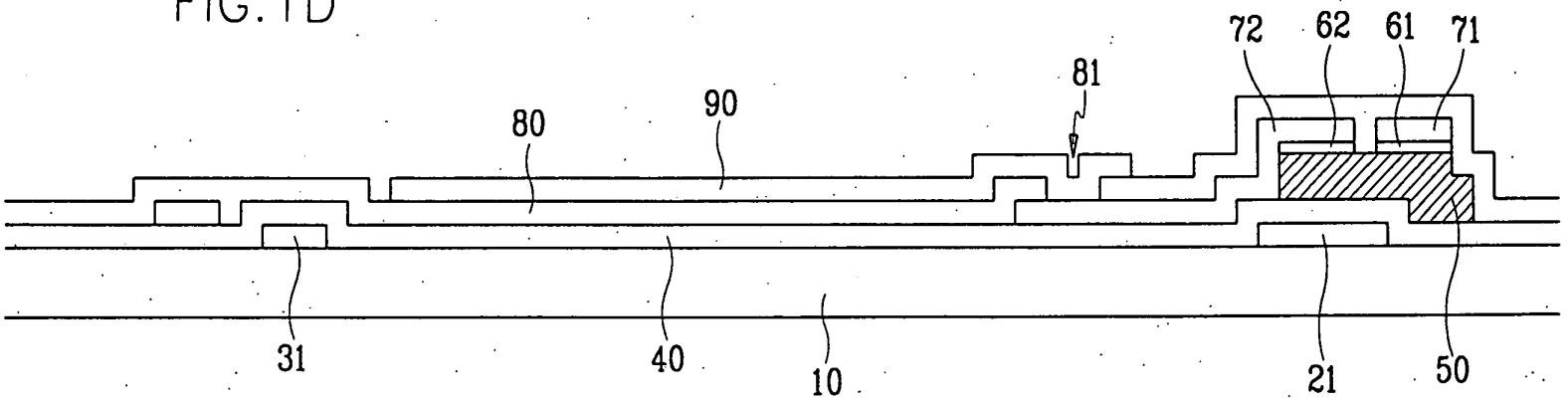


FIG. 1E

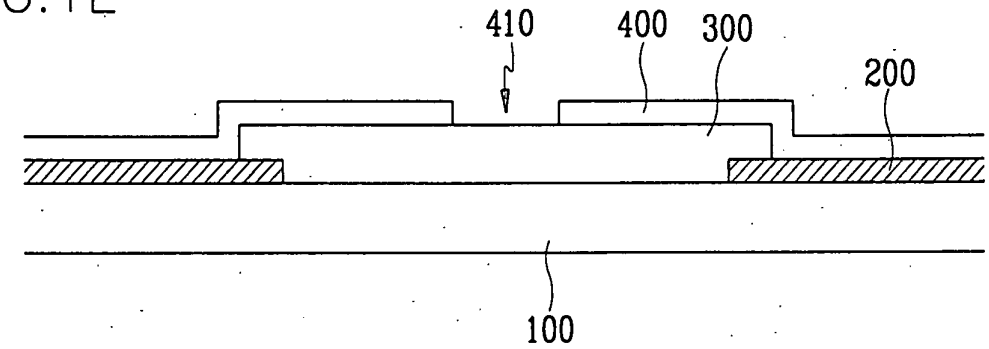


FIG. 1F

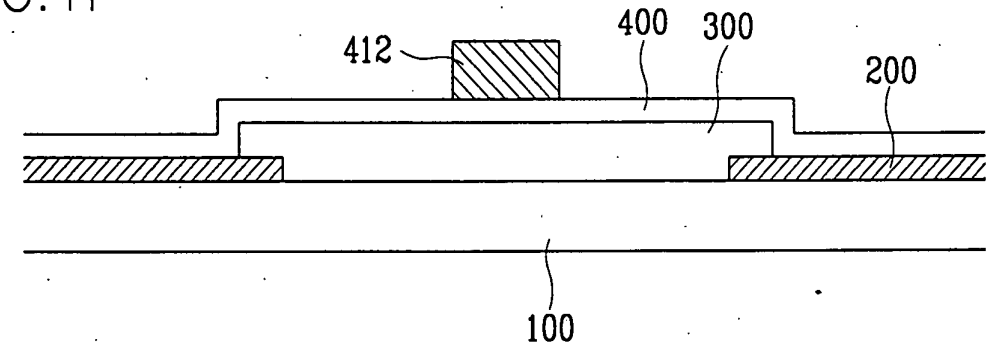


FIG.2A

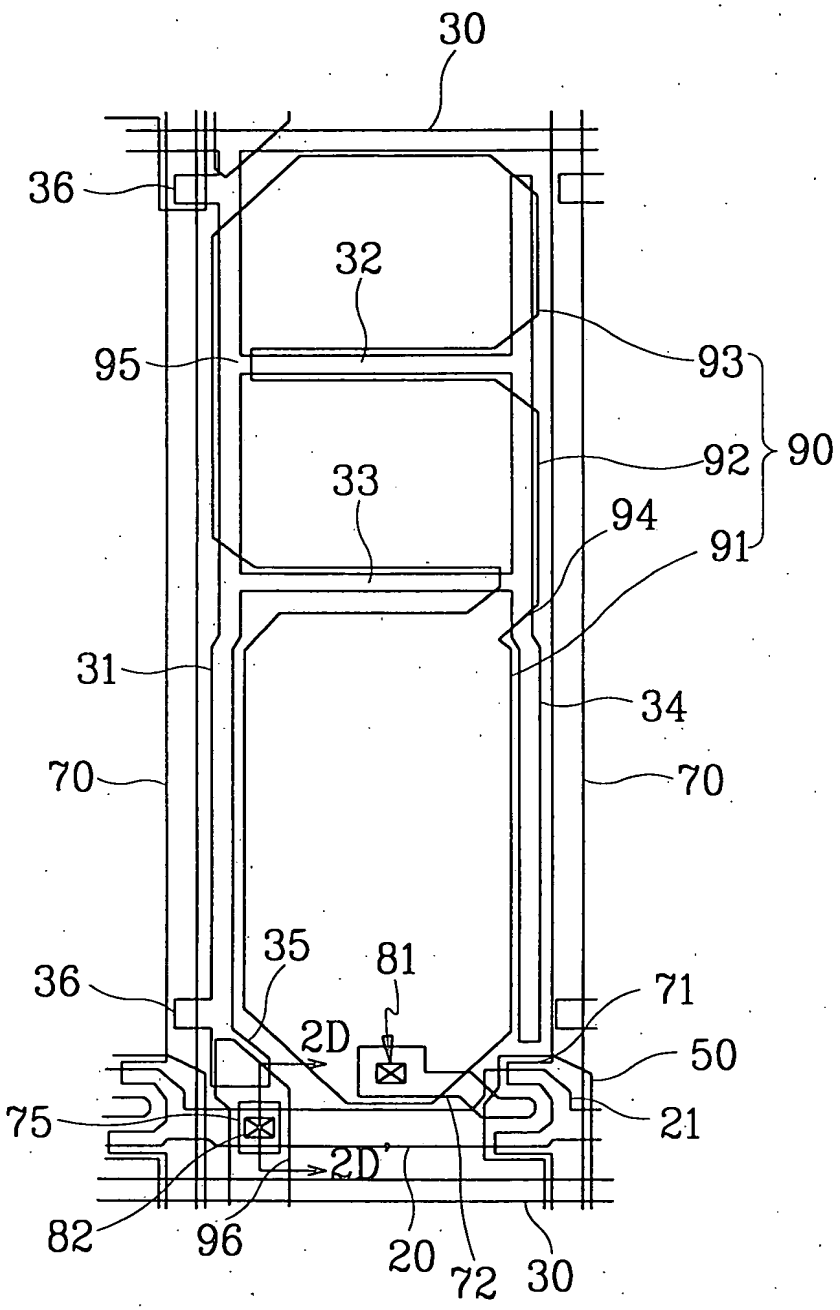

30
36
32
95
93
92
90
33
94
91
31
34
70
70
35
81
36
71
2D
50
75
21
2D'
82
96
20
72
30

FIG.2B

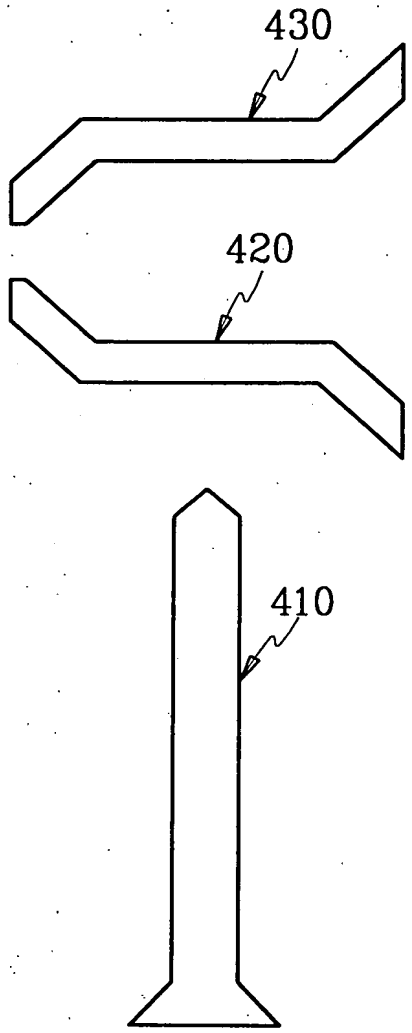


FIG.2C

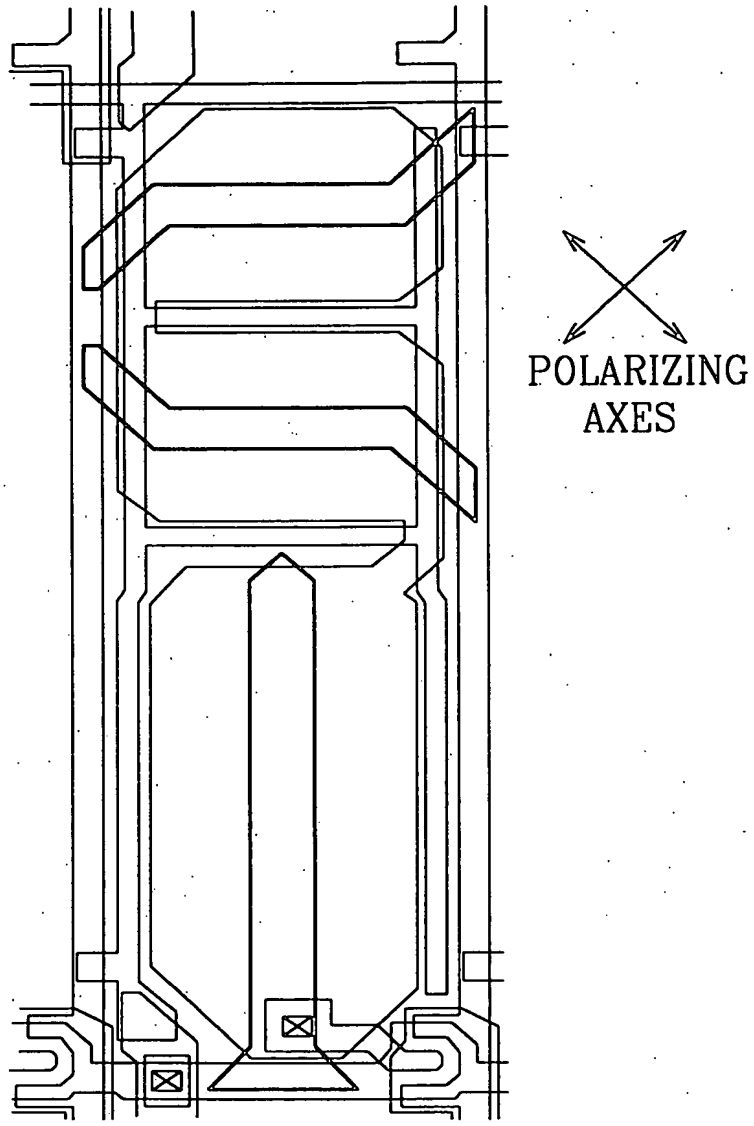


FIG.2D

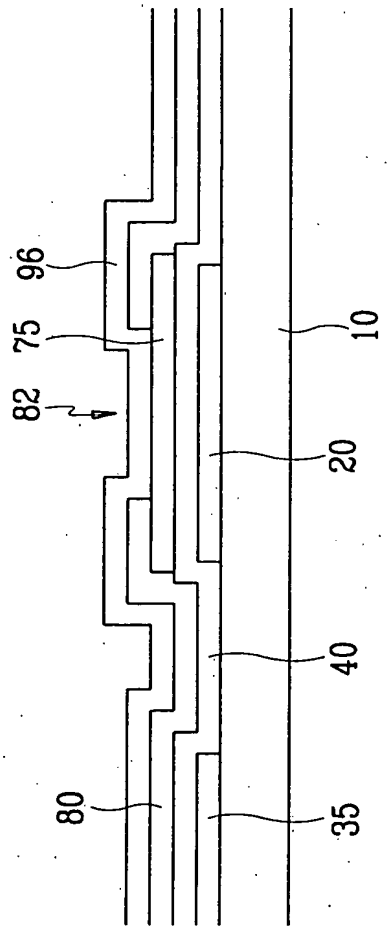


FIG.3A

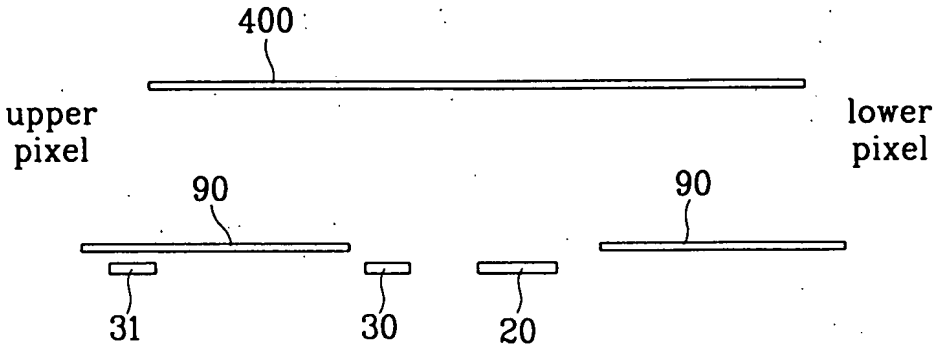


FIG.3B

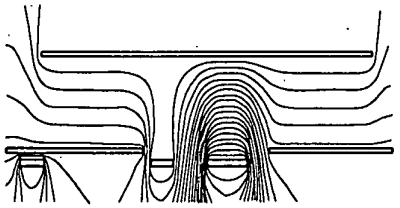
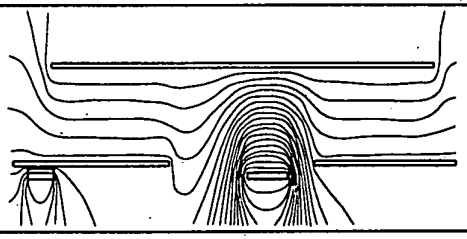
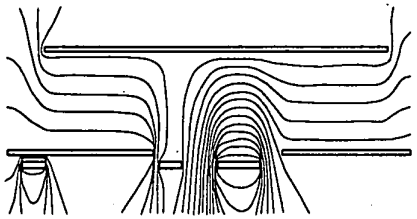
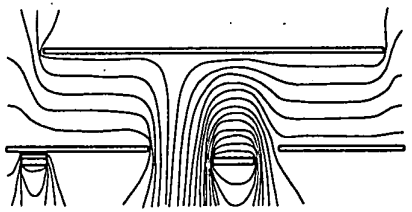
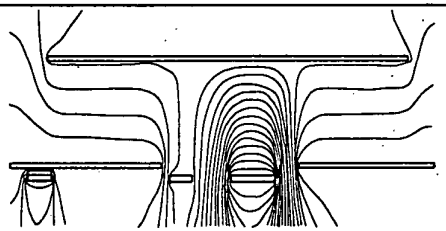
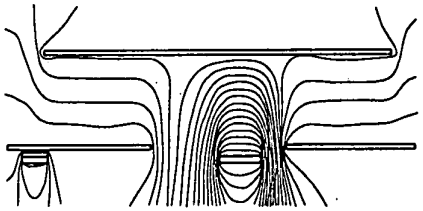
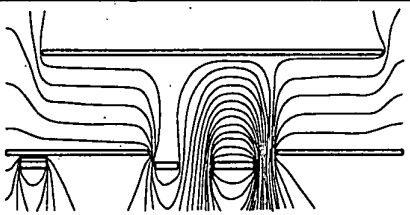
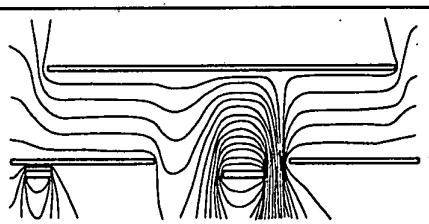
	TIME	POLARITY OF UPPER PIXEL	POLARITY OF LOWER PIXEL	WITH STORAGE ELECTRODE	WITHOUT STORAGE ELECTRODE
EXAMPLE 1	Gate ON	+	+		
	Gate OFF	+	−		
EXAMPLE 2	Gate ON	−	−		
	Gate OFF	−	+		

FIG.4A

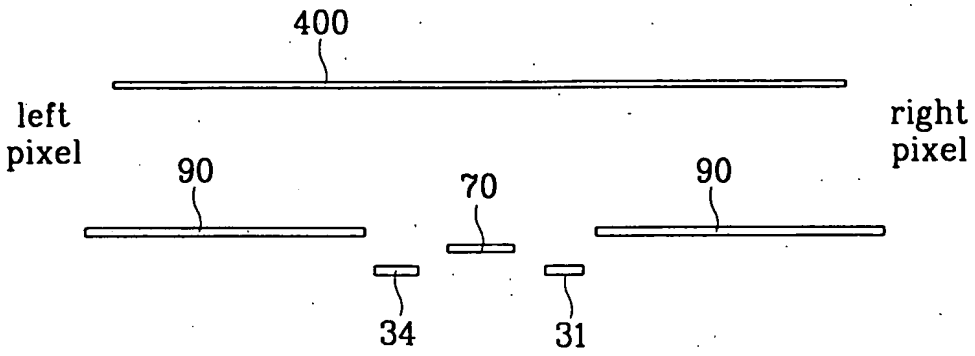
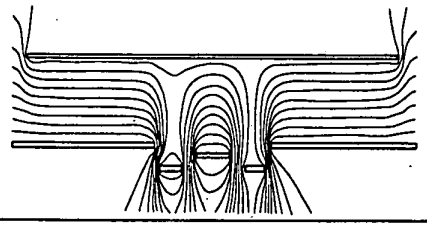
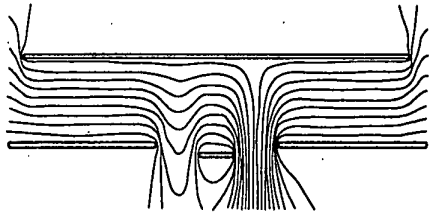
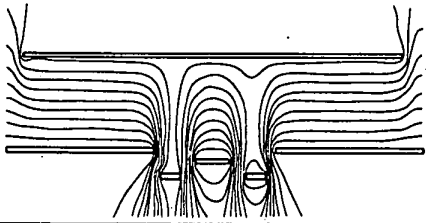
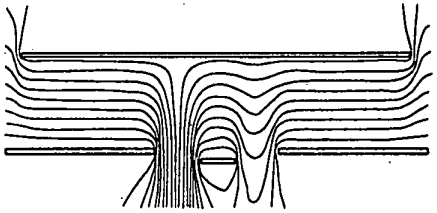
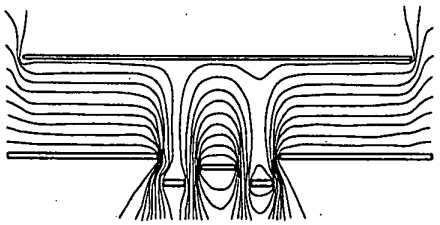
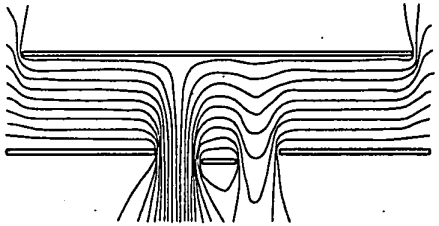


FIG.4B

	POLARITY OF LEFT PIXEL	POLARITY OF RIGHT PIXEL	POLARITY OF DATA LINE	WITH STORAGE ELECTRODE	WITHOUT STORAGE ELECTRODE
EXAMPLE 1	+	−	+		
			−		
EXAMPLE 2	−	+	+		
			−